AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Currently Amended) A method for forming interconnects in logic and memory devices on a single chip wherein the interconnects have an amorphous barrier layer on at least on three sides thereof, and wherein the method comprises

depositing an amorphous barrier layer of refractory metal nitride or carbide into a line or via hole by a vapor deposition technique, and

depositing a layer of a conductive metal having an average grain size of not smaller than 0.3 μm on top of said amorphous barrier layer filling said line or via hole; and

further comprising depositing a hard dielectric layer ~~between~~ in which said amorphous barrier layer and said conductive metal is formed.

4. (Original) A method for forming interconnects according to claim 3, wherein said refractory metal in said refractory metal nitride or carbide is selected form the group consisting of W, Ta and Ti.

5. (Original) A method for forming interconnects according to claim 3, wherein said conductive metal is selected from the group consisting of Cu, Ag, Al, CuAg, CuAl, AgAl and CuAgAl.

6. (Original) A method for forming interconnects according to claim 3, wherein said vapor deposition technique is a chemical vapor deposition technique.

7. (Original) A method for forming interconnects according to claim 3, wherein said refractory metal nitride is deposited by a chemical vapor deposition technique conducted at a reaction temperature about 300°C and about 400°C.

8. (Original) A method for forming interconnects according to claim 3, wherein said refractory metal nitride is deposited by a sputtering technique by using a composite target.

9. (Original) A method for forming interconnects according to claim 3 further comprising the step of annealing said amorphous barrier layer at a temperature of not lower than 400°C for at least ½ hour prior to the conductive metal deposition step.

10. (Original) A method for forming interconnects according to claim 3 further comprising the step of depositing a seed layer of said conductive layer prior to the conductive metal deposition step.

11. (Original) A method for forming interconnects according to claim 3, wherein said hard dielectric layer is deposited of a material selected from the group consisting of fluorinated oxide and amorphous or porous oxide treated with SiH_4 or CH_4.

12. (Canceled)

13. (Original) A method for forming interconnects in logic and memory devices on a single chip which comprises depositing a first layer of a soft metal containing grains having grain sizes sufficiently large so as to provide a substantially scratch-free surface upon polishing in a subsequent chemical mechanical polishing step and not less than 0.3μm; and further comprising depositing a layer of said soft metal containing grains having a grain size of not more than 50 nm and a layer thickness of not less than 400 nm prior to said deposition process of said first layer of soft metal so as to provide a substantially scratch-free surface upon polishing in a subsequent CMP step.

14. (Original) A method according to claim 13, wherein said first soft metal layer has a thickness of at least 100 nm.

15. (Original) A method according to claim 13 further comprising the steps of sequentially depositing a layer of Ti of less than 30 nm thick and a second layer of soft metal on top of said first soft metal layer such that the anti-electromigration property of said soft metal conductor is improved when said Ti layer is converted to $TiAl_3$ layer in a subsequent annealing process.

16. (Original) A method according to claim 13, wherein said soft metal is selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl, and CuAgAl.

17. (Original) The method according to claim 13 wherein said first layer of said soft metal is copper.

18. (Original) The method according to claim 13 wherein the layer thickness of the layer of said soft metal containing grains having a size of not more than 50 nm is not less than 600 nm.

19. (Original) The method according to claim 13 wherein the layer thickness of the layer of said soft metal containing grains having a size of not more than 50 nm is not less than 600 nm.

20. (Original) The method according to claim 13 which further comprises depositing said first layer and said second layer in openings located in low dielectric constant layer.

21. (Currently amended) A method for forming interconnects in logic and memory devices on a single chip wherein the interconnects have an amorphous barrier layer on at least on three sides thereof, and wherein the method comprises

depositing an amorphous barrier layer of refractory metal nitride or carbide into a line or via hole by a vapor deposition technique, and

depositing a layer of a conductive metal having an average grain size of not smaller than 0.3 μm on top of said amorphous barrier layer filling said line or via hole; and

further comprising providing a low-k dielectric layer ~~between~~ in which said amorphous barrier layer and said conductive meta is formed.